UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER OF PATENTS AND TRADEMARKS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/677,291	10/02/2000	Behnam Tabrizi	1920/107	4310

2101 7590 05/21/2003

BROMBERG & SUNSTEIN LLP
125 SUMMER STREET
BOSTON, MA 02110-1618

EXAMINER	
CHU, CHRIS C	

ART UNIT	PAPER NUMBER
2815	

DATE MAILED: 05/21/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/677,291	Applicant(s) TABRIZI, BEHNAM	
	Examiner Chris C. Chu	Art Unit 2815	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *05 March 2003* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1, 2, 4 - 22, 32, 34 - 36 and 40 - 48* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1, 2, 4 - 22, 32, 34 - 36 and 40 - 48* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☒ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Response to Amendment

1. Applicant's amendment field on March 5, 2003 has been received and entered in the case.

Claim Rejections - 35 USC § 112

2. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

3. Claim 47 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

In claim 47, it cannot be determined what applicant regards as "the electronic component may be used as a flip chip." Specifically, the phrase "may be used" renders the claim indefinite because it is unclear whether the limitation(s) following the phrase are part of the claimed invention.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 1, 2, 5 ~ 22, 32, 34 ~ 36 and 40 ~ 48 are rejected under 35 U.S.C. 103(a) as being unpatentable over Frei et al. in view of Kolesar, Jr.

Regarding claim 1, Frei et al. discloses in Fig. 9 and column 8, lines 8 ~ 12 an electronic component comprising:

- an electronic device package (12) formed from an integral substrate (38) having a recess (46), the recess including a conductive region (50); and
- a bare die electronic device (20) having a top, a bottom, sides, and a plurality of terminals (26 and 58), including a non-top terminal (58), the device being disposed in the recess, and wherein the non-top terminal is electrically coupled to the conductive region.

Frei et al. does not disclose the substrate to be silicon wafer. However, Kolesar, Jr. teaches in Fig. 5, Fig. 7E and column 6, lines 17 ~ 20 a substrate (500) to be silicon wafer. Thus, it would have been obvious to one of ordinary skill in the art at the time when the invention was made to modify Frei et al. by using the silicon wafer for the substrate as taught by Kolesar, Jr. The ordinary artisan would have been motivated to modify Frei et al. in the manner described above for at least the purpose of decreasing a thermal extension between the die and the substrate.

Regarding claim 2, Frei et al. discloses in Fig. 9 and column 7, line 22 the conductive region (50) being formed by metallization.

Regarding claim 5, Frei et al. discloses in Fig. 9 the device being physically coupled to the package by the conductive region.

Regarding claim 6, Frei et al. discloses in Fig. 9 a dielectric (a material in an area between top of 56 and top of 42) that is deposited so as to at least partially fill the recess.

Regarding claim 7, Frei et al. discloses in Fig. 9 and Fig. 11 a plurality of metallized bumps (60 and 62) in a plane, wherein each terminal is electrically coupled to at least one bump, and each bump is electrically coupled to at most one electrically distinct terminal (70).

Regarding claim 8, Frei et al. discloses in Fig. 9 the package (12) including a top and a bottom; and the bumps are located above the top of the package.

Regarding claim 9, Frei et al. discloses in Fig. 9 the device (20) being a vertical device and the bottom of the device is coupled to the package in the recess.

Regarding claim 10, Frei et al. discloses the claimed invention except for a second conductive region coupled to a terminal other than the non-top terminal. However, Kolesar, Jr. teaches in Fig. 7E a second conductive region (Aluminum Film) coupled to a terminal other than the non-top terminal. Thus, it would have been obvious to one of ordinary skill in the art at the time when the invention was made to further modify Frei et al. by using the second conductive region to be coupled to a terminal other than the non-top terminal as taught by Kolesar, Jr. The ordinary artisan would have been motivated to further modify Frei et al. in the manner described above for at least the purpose of providing the realization of complex integrated circuit die interconnect schemes which emulate the technology of multiple layer printed circuit boards in flexibility (column 15, lines 26 ~ 39).

Regarding claim 11, Frei et al. discloses in Fig. 9 a plurality of contact including at least a first contact (60) and a second contact (62), the first contact being electrically coupled to the non-top terminal and the second contact being electrically coupled to a terminal other than the non-top terminal.

Regarding claim 12, Frei et al. discloses in Fig. 9 the plurality of contacts reside in the same plane.

Regarding claim 13, Frei et al. discloses the claimed invention except for a second layer of dielectric completely covering the silicon wafer and the device except for the plurality of contacts. However, Kolesar, Jr. teaches in Fig. 7B a second layer of dielectric (704) completely covering the silicon wafer and the device except for the plurality of contacts. Thus, it would have been obvious to one of ordinary skill in the art at the time when the invention was made to further modify Frei et al. by using the second layer of dielectric as taught by Kolesar, Jr. The ordinary artisan would have been motivated to further modify Frei et al. in the manner described above for at least the purpose of protecting the die.

Regarding claim 14, Frei et al. discloses in Fig. 9, Fig. 10 and column 8, lines 8 ~ 12 an electronic component comprising:

- an electronic component package (12) formed from an integral substrate (38) having a recess (46), the recess including a first conductive region (50); and
- a bare die electronic device (20) having a top, a bottom, sides, and a plurality of terminals (26 and 58), including a non-top terminal and a top terminal (58), the device being disposed in the recess, wherein the non-top terminal is electrically coupled to the first conductive region (50, at the right) and a second conductive region (50, at the

left), and wherein at least a portion of the first and second conductive regions are essentially planar.

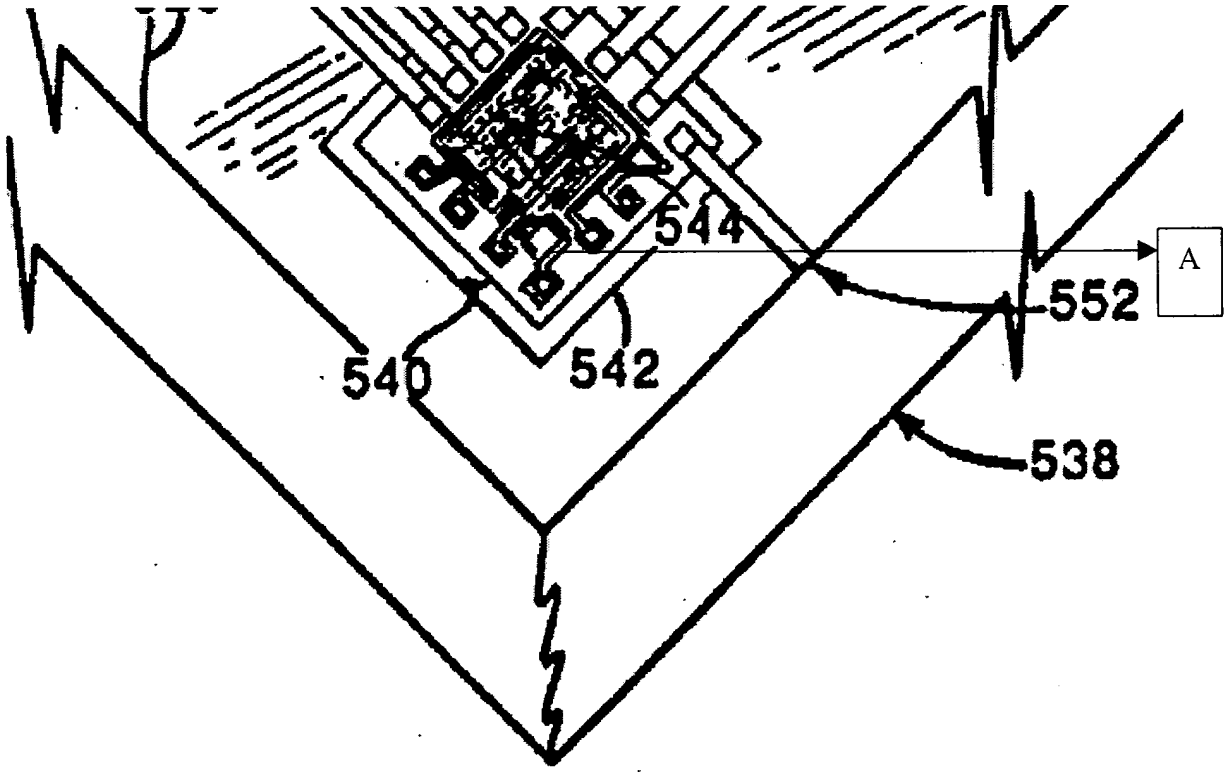
Frei et al. does not disclose the substrate to be silicon wafer and an electrical connection between the top terminal and a second conductive region. However, Kolesar, Jr. teaches in Fig. 5 and column 6, lines 17 ~ 20 a substrate (500) to be silicon wafer and an electrical connection (A in Fig. 5 of this Office action, see next page) between the top terminal and the second conductive region. Thus, it would have been obvious to one of ordinary skill in the art at the time when the invention was made to modify Frei et al. by using the silicon wafer for the substrate and the electrical connection as taught by Kolesar, Jr. The ordinary artisan would have been motivated to modify Frei et al. in the manner described above for at least the purpose of decreasing a thermal extension between the die and the substrate.

Regarding claim 15, Frei et al. discloses in Fig. 10 the second conductive region being a solder bump (62).

Regarding claim 16, Frei et al. discloses in Fig. 9, Fig. 10 and column 8, lines 8 ~ 12 an electronic component comprising:

- an electronic component package (12) formed from an integral substrate (38) having a recess (46), the recess including a first conductive region (50); and
- an electronic device (20) having a top, a bottom, sides, and a plurality of terminals (26 and 58), including a non-top terminal (58) located in a region other than the top of the device, the device being disposed in the recess, wherein the non-top terminal is electrically coupled to the conductive region.

Frei et al. does not disclose the substrate to be silicon wafer. However, Kolesar, Jr. teaches in Fig. 5, Fig. 7E and column 6, lines 17 ~ 20 a substrate (500) to be silicon wafer. Thus, it would have been obvious to one of ordinary skill in the art at the time when the invention was made to modify Frei et al. by using the silicon wafer for the substrate as taught by Kolesar, Jr. The ordinary artisan would have been motivated to modify Frei et al. in the manner described above for at least the purpose of decreasing a thermal extension between the die and the substrate.



Wafer Scale Intergration Assembly

Fig. 5

Regarding claim 17, Frei et al. discloses in Fig. 9 one of the terminals (26) of the device (20) being a top contact located at the top of the device; and the package (12) having a package top, wherein the package top also including a contact (62) coupled electrically via the conductive region to the non-top terminal.

Regarding claim 18, Frei et al. discloses in Fig. 9 and column 7, line 22 the conductive region (50) comprising a layer of metal; and the electronic device (12) resides within the recess and the metal is electrically coupled to the non-top terminal of the device.

Regarding claim 19, Frei et al. discloses the claimed invention except for a layer of insulation coupling the silicon package to the electronic device. However, Kolesar, Jr. teaches in Fig. 6C a layer of insulation (604) coupling the silicon package to the electronic device. Thus, it would have been obvious to one of ordinary skill in the art at the time when the invention was made to further modify Frei et al. by using the insulation layer as taught by Kolesar, Jr. The ordinary artisan would have been motivated to further modify Frei et al. in the manner described above for at least the purpose of protecting the die.

Regarding claim 20, Frei et al. discloses in Fig. 9 the metal of the conductive region (50) extending to a portion of the package top, the electronic component further comprising: a bottom contact electrically coupled to the metal on the package top.

Regarding claim 21, Frei et al. discloses in Fig. 9, Fig. 10 and column 8, lines 8 ~ 12 and lines 33 ~ 42 an electronic component comprising:

- an electronic device (20) having a first terminal (26) and a second terminal (58), wherein a first dimension is defined therebetween;

- an electronic device package (12) having a first surface, the package formed from an integral substrate (38) having a recess (46) on the first surface that has a depth that is substantially equal to the first dimension, the package further having a layer of metal (50) applied to the recess and to a portion of the first surface, wherein the electronic device resides within the recess and the second terminal is coupled to the layer of metal.

Frei et al. does not disclose the substrate to be silicon wafer and an insulation layer. However, Kolesar, Jr. teaches in Fig. 5, Fig. 6C, Fig. 7E and column 6, lines 17 ~ 20 a substrate (500) to be silicon wafer and a layer of insulation (604) coupling the electronic device to the silicon wafer. Thus, it would have been obvious to one of ordinary skill in the art at the time when the invention was made to modify Frei et al. by using the silicon wafer for the substrate and the insulation layer as taught by Kolesar, Jr. The ordinary artisan would have been motivated to modify Frei et al. in the manner described above for at least the purpose of decreasing a thermal extension between the die and the substrate.

Regarding claim 22, Frei et al. discloses in Fig. 9 a first contact (60) coupled to the first terminal (26); and a second contact (62) coupled to the metal (50) residing on the first surface of the package.

Regarding claim 32, Frei et al. discloses in Fig. 9, Fig. 10 and column 8, lines 8 ~ 12 an electronic component comprising:

- a non-molded electronic component package (12) having a package top and from an integral substrate (38) including a recess (46);

- a planar bare die electronic device (20) having a top, a bottom, sides, and a plurality of contacts (26 and 58), the device being disposed in the recess.

Frei et al. does not disclose the substrate to be silicon wafer and a planarizing material. However, Kolesar, Jr. teaches in Fig. 5, Fig. 6C and column 6, lines 17 ~ 20 a substrate (500) to be silicon wafer and a planarizing material (604) filling the recess not occupied by the device to substantially create a level plane that includes the package top. Thus, it would have been obvious to one of ordinary skill in the art at the time when the invention was made to modify Frei et al. by using the silicon wafer for the substrate and the planarizing material as taught by Kolesar, Jr. The ordinary artisan would have been motivated to modify Frei et al. in the manner described above for at least the purpose of decreasing a thermal extension between the die and the substrate.

Regarding claim 34, Frei et al. discloses in Fig. 9 a metallization layer (50).

Regarding claim 35, Frei et al. discloses in Fig. 9 the metallization layer couples each contact to a redistribution point on the package top, and each contact remains electrically distinct.

Regarding claim 36, Frei et al. discloses in Fig. 9 a plurality of conductive bumps (62), each bump being disposed at a redistribution point.

Regarding claim 40, Frei et al. discloses in Fig. 9, Fig. 10 and column 8, lines 8 ~ 12 an electronic component comprising:

- an electronic device package (12) including a substrate (38) having a recess (46), the recess including a conductive region (50); and

- a bare die electronic device (20) having a top, a bottom, sides, and a plurality of terminals (26 and 58), including a non-top terminal (58), the device being disposed in the recess, and wherein the non-top terminal is electrically coupled to the conductive region.

Further, the limitation "by non-wire bonding" is product-by-process claim. Even though product-by-process claim is limited by and defined by the process, determination of patentability is based upon the product itself. The patentability of a product does not depend on its method of production. If the product in product-by-process claim is the same as or obvious from a product of the prior art, the claim is unpatentable even though the prior product is made by a different process. In re Thorpe, 227 USPQ 964, 966 (Fed. Cir. 1985) (citations omitted). A "product by process" claim is directed to the product per se, no matter how actually made, In re Hirao, **190 USPQ 15 at 17** (footnote 3). See also In re Brown, **173 USPQ 685**: In re Luck, **177 USPQ 523**; In re Fessmann, **180 USPQ 324**: In re Avery, **186 USPQ 116**; In re Wertheim, **191 USPQ 90 (209 USPQ 254** does not deal with this issue); and In re Marosi et al., **218 USPQ 289** final product per se which must be determined in a "product by, all of" claim, and not the patentability of the process, and that an old or obvious product, whether claimed in "product by process" claims or not. Note that Applicant has the burden of proof in such cases, as the above caselaw makes clear.

Frei et al. does not disclose the substrate to be silicon wafer. However, Kolesar, Jr. teaches in Fig. 5, Fig. 7E and column 6, lines 17 ~ 20 a substrate (500) to be silicon wafer. Thus, it would have been obvious to one of ordinary skill in the art at the time when the invention was

made to modify Frei et al. by using the silicon wafer for the substrate as taught by Kolesar, Jr. The ordinary artisan would have been motivated to modify Frei et al. in the manner described above for at least the purpose of decreasing a thermal extension between the die and the substrate.

Regarding claim 41, Frei et al. discloses in Fig. 9 the second conductive region. Further, the limitation "by non-wire bonding" is product-by-process claim. Even though product-by-process claim is limited by and defined by the process, determination of patentability is based upon the product itself. The patentability of a product does not depend on its method of production. If the product in product-by-process claim is the same as or obvious from a product of the prior art, the claim is unpatentable even though the prior product is made by a different process. In re Thorpe, 227 USPQ 964, 966 (Fed. Cir. 1985) (citations omitted). A "product by process" claim is directed to the product per se, no matter how actually made, In re Hirao, **190 USPQ 15 at 17** (footnote 3). See also In re Brown, **173 USPQ 685**: In re Luck, **177 USPQ 523**; In re Fessmann, **180 USPQ 324**: In re Avery, **186 USPQ 116**; In re Wertheim, **191 USPQ 90 (209 USPQ 254** does not deal with this issue); and In re Marosi et al., **218 USPQ 289** final product per se which must be determined in a "product by, all of" claim, and not the patentability of the process, and that an old or obvious product, whether claimed in "product by process" claims or not. Note that Applicant has the burden of proof in such cases, as the above caselaw makes clear.

Regarding claim 42, Kolesar, Jr. discloses in Fig. 6C and column 11, lines 9 and 10 the layer (604) being a dielectric.

Regarding claim 43, Frei et al. discloses in Fig. 11 the conductive bumps (62) being spaced for electrically coupling with a pre-printed circuit board (68).

Regarding claim 44, Frei et al. discloses in Fig. 11 the electronic component being a flip chip.

Regarding claim 45, Frei et al. discloses in Fig. 9, Fig. 10 and column 8, lines 8 ~ 12 an electronic component comprising:

- a substrate (38) having a recess (46);
- a bare die electronic device (20) having at least one contact (26 and 58), the device being disposed in the recess; and
- an electrically conductive material (56) coupling the at least one contact (58) to an electrical input (62) of the electronic component.

Further, the limitation "wherein the electrical coupling is achieved by non-wire bonding" is product-by-process claim. Even though product-by-process claim is limited by and defined by the process, determination of patentability is based upon the product itself. The patentability of a product does not depend on its method of production. If the product in product-by-process claim is the same as or obvious from a product of the prior art, the claim is unpatentable even though the prior product is made by a different process. In re Thorpe, 227 USPQ 964, 966 (Fed. Cir. 1985) (citations omitted). A "product by process" claim is directed to the product per se, no matter how actually made, In re Hirao, **190 USPQ 15 at 17** (footnote 3). See also In re Brown, **173 USPQ 685**: In re Luck, **177 USPQ 523**; In re Fessmann, **180 USPQ 324**: In re Avery, **186 USPQ 116**; In re Wertheim, **191 USPQ 90 (209 USPQ 254** does not deal with this

issue); and In re Marosi et al., **218 USPQ 289** final product per se which must be determined in a "product by, all of" claim, and not the patentability of the process, and that an old or obvious product, whether claimed in "product by process" claims or not. Note that Applicant has the burden of proof in such cases, as the above caselaw makes clear.

Frei et al. does not disclose the substrate to be silicon wafer. However, Kolesar, Jr. teaches in Fig. 5, Fig. 7E and column 6, lines 17 ~ 20 a substrate (500) to be silicon wafer. Thus, it would have been obvious to one of ordinary skill in the art at the time when the invention was made to modify Frei et al. by using the silicon wafer for the substrate as taught by Kolesar, Jr. The ordinary artisan would have been motivated to modify Frei et al. in the manner described above for at least the purpose of decreasing a thermal extension between the die and the substrate.

Regarding claim 46, Frei et al. discloses the claimed invention except for at least one layer of dielectric. However, Kolesar, Jr. teaches in Fig. 6C at least one layer of dielectric (604) that resides within the recess of the silicon wafer that is not taken up by the bare die electronic device. Thus, it would have been obvious to one of ordinary skill in the art at the time when the invention was made to further modify Frei et al. by using at least one layer of dielectric as taught by Kolesar, Jr. The ordinary artisan would have been motivated to further modify Frei et al. in the manner described above for at least the purpose of protecting the die.

Regarding claim 47, Frei et al. and Kolesar, Jr. discloses the bare die electronic device being covered by the dielectric material and the electronic component may be used as a flip chip.

Regarding claim 48, Kolesar, Jr. discloses in Fig. 5, Fig. 7E and column 6, lines 17 ~ 20 the silicon wafer (500) being an integral piece of silicon.

6. Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over Frei et al. and Kolesar, Jr. as applied to claim 1 above, and further in view of Yoshida et al. or Oji et al.

Frei et al. and Kolesar, Jr. discloses the claimed invention except the conductive region comprises: a first layer of titanium; a second layer of copper deposited on the first layer; and a third layer of chrome deposited on the second layer. However, Yoshida et al. or Oji et al. discloses the conductive region comprises: a first layer of titanium; a second layer of copper deposited on the first layer; and a third layer of chrome deposited on the second layer. Thus, it would have been obvious to one of ordinary skill in the art at the time when the invention was made to further modify Frei et al. and Kolesar, Jr. by adding the conductive region as taught by Yoshida et al. or Oji et al. The ordinary artisan would have been motivated to further modify Frei et al. and Kolesar, Jr. in the manner described above for at least the purpose of increasing adhesive strength between the conductive region and the device.

Response to Arguments

7. Applicant's arguments with respect to claims 1, 14, 16, 18, 21 and 32 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

8. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Chris C. Chu whose telephone number is (703) 305-6194. The examiner can normally be reached on M-F (10:30 - 7:00).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie C. Lee can be reached on (703) 308-1690. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 308-7382 for regular communications and (703) 308-7722 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

Chris C. Chu
Examiner
Art Unit 2815

c.c.
May 13, 2003

ALLAN R. WILSON
PRIMARY EXAMINER